REMARKS

Claims 7-12 are pending in the present application. In the outstanding Office Action, claims 7-9 have been rejected under 35 U.S.C. § 102(b), and claims 10-12 have been rejected under 35 U.S.C. § 103.

In the Amendment submitted herein, claim 7 is amended. No new matter has been introduced as support for the amendment is found in the originally filed claims, specification and drawings. Entry of the amendment is respectfully requested.

Claims 7-9 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kikuo, et al. (EP 634 797 A2). "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631, 2 SPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, "[t]he identical invention must be shown in as complete detail as is contained in the * * * claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The Examiner states that Kikuo discloses in Figure 17 a thin film transistor comprising a semiconductor film 102, a first gate insulating film 103, a second gate insulating film 104 and a gate electrode G as recited in claim 7. Applicant respectfully submits that the anticipation rejection of claims 7-9 is improper because Kikuo fails to teach each and every element as recited in claim 7.

Claim 7, as amended, includes a thin film transistor comprising a semiconductor film, a first gate insulating film, a second gate insulating film and a gate electrode sequentially formed in that order on one major surface of a substrate. The first gate insulating film is recited as covering the major surface of the substrate and all regions of the semiconductor film other than a

contact region, and the second gate insulating film is recited as being made of a material for supplying hydrogen to the semiconductor film and being formed only in a region covered by the gate electrode to have substantially the same shape as the gate electrode.

In the Kikuo reference, the first gate insulating film 103 is not formed to cover the one major surface of the substrate and all regions of the semiconductor film other than a contact region. Instead, Figure 17 of Kikuo teaches that the gate insulating film 103 only covers the region where the polycrystalline silicon film 102 is formed. The gate insulating film 103 does not cover the substrate 101. Accordingly, the Kikuo reference does not anticipate claim 7. In addition, because claims 8-9 include all of the limitations of claim 7, Kikuo does not anticipate claims 8-9. For at least the foregoing reasons, the anticipation rejection of claims 7-9 based on the Kikuo reference is improper, thus reconsideration and withdrawal thereof are respectfully requested.

Claims 7-9 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kaganowicz et al. (U.S. Patent No. 4,692,344). "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631, 2 SPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, "[t]he identical invention must be shown in as complete detail as is contained in the * * * claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The Examiner states that Kaganowicz et al. discloses a semiconductor device comprising a semiconductor film 44, a first gate insulating film 48, a second gate insulating film 50 and a gate electrode 52 as recited in claim 7.

However, the first gate insulating film 48 does not cover the one major surface of the substrate and all regions of the semiconductor film other than a contact region as recited in claim

7, as amended. Instead, Kaganowicz et al. teaches and suggests that the first gate insulating film 48 is formed to have a same shape as that of the second gate insulating film 50 and the electrode 52.

In light of the foregoing, Kaganowicz does not disclose each and every element as recited in claim 7. Therefore, claim 7 is not anticipated by Kaganowicz. For at least the same reasons applied to claim 7, claims 8-9 are not anticipated by Kaganowicz. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 7-9 under 35 U.S.C. § 102(b).

Claims 10-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kikuo in view of Takemura, et al. (U.S. Patent No. 5,719,065). For an obviousness rejection to be proper, the Examiner must meet the burden of establishing that all elements of the invention are disclosed in the prior art. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988).

The Examiner alleges that Kikuo discloses a thin film transistor comprising a semiconductor film 102, a first gate insulating film 103, a second gate insulating film 104 and a gate electrode G formed on a surface of substrate 101, wherein the first gate insulating film covers the semiconductor film, and the second gate insulating film is made of a material for supplying hydrogen to the semiconductor film. The Examiner alleges that Takemura discloses, in Figure 2D, a gate insulating film 6 with a smaller film thickness in a region not covered with a gate electrode 7 than that in a region covered with the gate electrode.

First, Kikuo and Takemura do not teach or suggest all of the limitations of claim 10. Takemura does not disclose provisions of **a two-layer structured gate insulating film** at the region where the gate electrode and the channel region overlap. Applicant's claim 10 provides that "**said second gate insulating film** is made of a material for supplying hydrogen to said

semiconductor film and has a smaller film thickness in a region not covered with said gate electrode than that in a region covered with said gate electrode." (Emphasis supplied.)

The Examiner attempts to combine Kikuo, which has the two layered structure gate, with Takemura, which only has the single layer structured gate, to obtain all of the limitations of claim 10. However, as claimed in claim 10, it is the **second** gate insulating film that has a smaller film thickness in a region not covered with the gate electrode than that in a region covered with the gate electrode. In addition, the second gate insulating film is recited as being made of a material for supplying hydrogen to the semiconductor film. Thus, because Takemura does not have a two layer structure gate, Kikuo and Takemura do not teach or suggest the limitations of claim 10.

Moreover, there is no motivation to combine the single layer structure gate of Takemura with Kikuo. The structure as recited in claim 10 provides certain advantages that are not taught or suggested by either Kikuo or Takemura. In particular, claim 10 has the advantage of blocking intrusion of the impurities at the second gate insulating film, in addition to the blockage of intrusion of impurities at the first gate insulating film. By having a two layered structure gate, the second gate insulating film can also function as a hydrogen source for hydrogenation of the semiconductor film. In addition, by having the thickness of the **second** gate insulating film smaller in a region not covered with the gate electrode, sufficient ion doping can be achieved at low energy through the second and first insulating films, to thereby improve reliability of the TFT. It is also possible to maintain the energy at a low level for ion doping performed through the gate insulating films, to reliably perform hydrogenation to at least the channel region of the thin film transistor, and to reliably prevent intrusion of contamination materials to the semiconductor film. Thus, there are simultaneous advantages to having the **second** gate insulating film smaller in a region not covered with the gate electrode.

Because Takemura is only a single layered structure gate, Takemura does not and cannot teach the simultaneous advantages that occur as a result of the structure recited in claim 10. In contrast, Takemura teaches forming the charge trapping layer to be in direct contact with the source and drain region 1 and 5. Further, Takemura teaches forming the gate insulating film 6 in a thin thickness in order that the influence of positive charges in the trapping layer 11 extends to the high resistivity region 3 (column 3, lines 44-47). In this respect, the gate insulating film 6 of Takemura does not correspond to the second gate insulating film as recited in claim 10. In addition, because Kikuo does not have a thickness of the **second** gate insulating film smaller in a region not covered with the gate electrode; thus, Kikuo does not and cannot teach the simultaneous advantage that occur as a result of the structure recited in claim 10. Neither Kikuo nor Tademura teaches or suggests the modification as suggested by the Examiner.

Moreover, there is no reasonable expectation of success in combining the teachings of the references to make the claimed invention. As discussed above, the references clearly lack the structural relationship among first and second gate insulating films, a gate electrode and a semiconductor film, which enables hydrogenation to the semiconductor, particularly to the channel region, and prevention of intrusion of contamination impurities. Also, when considering the function and structure of the charge trapping layer 11 taught by Takemura, there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference teachings to make the claimed invention.

For at least the foregoing reasons, a *prima facie* obviousness does not exist with regard to claim 10. Accordingly, claim 10 is not rendered obvious by Kikuo and Takemura. For at least the same reasons, claims 11-12 allowable as depending from claim 10. Reconsideration and withdrawal of the rejection of claims 10-12 under 35 U.S.C. § 103 are respectfully requested.

In conclusion, claims 7-12 are not anticipated nor rendered obvious because all the limitations of the claimed invention are not taught or suggested by the references, individually or in combination. Therefore, the anticipation rejection of claims 7-9 and the obviousness rejection of claims 10-12 are improper, thus reconsideration and withdrawal thereof are respectfully requested.

It is believed that the foregoing amendments and remarks fully comply with the Office Action and that the claims are allowable to Applicant. Accordingly, reconsideration and allowance is requested.

The Examiner is invited to contact Applicants' Attorneys at the below-listed telephone number regarding this Amendment or otherwise regarding the present application.

If there are any fees with respect to this Amendment or otherwise, please charge them to Deposit Account No. 06-1130 maintained by Applicants' attorneys.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claim 7 is amended in "marked up" format, as follows.

7. (Amended/Marked up) A thin film transistor comprising a semiconductor film, a first gate insulating film, a second gate insulating film and a gate electrode sequentially formed in that order on one major surface of a substrate,

wherein said first gate insulating film covers said one major surface of the substrate and all regions of said semiconductor film other than a contact region, and

said second gate insulating film is made of a material for supplying hydrogen to said semiconductor film and is formed only in a region covered by said gate electrode to have substantially the same shape as said gate electrode.